Logic Synthesis Using Synopsys 2nd Edition

basic synthesis flow and commands - bgu *- logic synthesis page 65 introduction to digital vlsi link library • the link library is a technology library that is used to describe the function of mapped cells prior to optimization.* ***design compiler ug: 3. working with design files*** *- home contents index / 3-1 v1999.10 design compiler user guide 3 working with design files 3 designs are stored in design files, which are ascii files containing a* ***state machine coding styles for synthesis - sunburst design*** *- snug 1998 state machine coding styles for synthesis rev 1.1 2 introduction steve golson's 1994 paper, "state machine design techniques for verilog and vhdl" [1], is a* ***nonblocking assignments in verilog synthesis, coding ...*** *- snug san jose 2000 nonblocking assignments in verilog rev 1.4 synthesis, coding styles that kill 4 4.0 nonblocking assignments the nonblocking assignment operator is the same as the less-than-or-equal-to operator ("*